HuC6280

CMOS Programmable Sound Generator

MANUAL

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1. DESCRIPTION

Programmable sound generator (PSG) is a sub-block of the HuC6280 LSI. By waveform memory method, it generates various sorts of sound under software control. It has two noise generators which provide rhythm or sound effects, and a low-frequency oscillator which generates special sound effects (ex. UFO sound) or effect of vibrato.

1.1 Features

- Monolithic CMOS programmable sound generator
- Sound generation..... waveform memory method (32 words for a cycle)
- Number of channels, generators..... Six channels for waveform/sound generation, and two of them are selective for square waveform noise or sound generation
- Combination of waveform generator and noise generator..... Six sound sources configuration to four sound sources + two noise sources configuration
- Amplitude level control ..... Wide dynamic range control by using 5-bit logarithmic conversion technique
- Stereo output
- Real sound output (direct D/A (DDA) mode)
- On-chip low frequency oscillator (LFO)
- Single power supply..... 5V
- 80-pin plastic flat package

2. FUNCTIONS

All PSG functions are controlled by the data written in the registers in the PSG block. In other words, sound is generated from the PSG according to the contents of each register. (This does not apply to the direct D/A (DDA) mode.)

- Waveform generator (ch.1-ch.6) : Generates waveforms of each channel according to the contents of the waveform register (5 bits × 32 words for a cycle).
- Noise generator (ch.5, ch.6) : Generates pseudo random noise (square wave).
- Amplitude level control : Controls the amplitude level of mixed Left/Right output, according to the data stored in registers.
- Low-frequency oscillator : Generates a low frequency for modulation. It uses the waveform from channel 2 to modulate the sound of channel 1.

2.1 Register Functions

Each channel of the PSG has registers R2 – R7 in the table below. A register is addressed by the conbination of A0 – A3 and R0. R0, R1, R8 and R9 are addressed by the combination of A0 – A3.

There are one R0, one R1, one R8 and one R9 in the PSG block.

Ch5 and ch6 have R7 individually.

Registers		D7	D6	D5	D4	D3	D2	D1	D0	
R0	Channel select						ch SEL			* One for all channels
R1	Main amplitude level adjustment	LMAL				RMAL				
R2	Lower order of frequency	FRQ LOW								* Each channel has all of these registers, except R7 which is provided for channel 5 and 6 only.
R3	Higher order of frequency					FRQ HIGH				
R4	Channel on, DDA, channel amplitude level	ON	DDA		AL					
R5	L/R amplitude level	LAL				RAL				
R6	Waveform				WAVE DATA					
R7	Noise enable, noise frequency	NE			NOISE FRQ					
R8	LFO frequency	LFO FRQ								* One for all channels
R9	LFO control	LF TRG						LF CTL		

The relation between the A0 – A3 values and the registers is shown in the table below. (A0 = LSB and A3 = MSB)

A0 – A3 (hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Registers	R0	R1	R2	R3	R4	R5	R6	R7	R8	R9						

The following lists all the registers contained in the PSG.

	ch1	ch2	ch3	ch4	ch5	ch6
R0	Only one for PSG } (R0 is not affective)			ch (annel) SELECT		
R1	Only one for PSG }			M(ain) A(mplitude Level) (LMAL, RMAL)		
R2	FRQ LOW	FRQ LOW	FRQ LOW	FRQ LOW	FRQ LOW	FRQ LOW
R3	FRQ HI	FRQ HI	FRQ HI	FRQ HI	FRQ HI	FRQ HI
R4	ON DDA AL	ON DDA AL	ON DDA AL	ON DDA AL	ON DDA AL	ON DDA AL
R5	LAL RAL	LAL RAL	LAL RAL	LAL RAL	LAL RAL	LAL RAL
R6	WAVE DATA	WAVE DATA	WAVE DATA	WAVE DATA	WAVE DATA	WAVE DATA
R7					NE NOISE FRQ	NE NOISE FRQ
R8	Only one for PSG } (R0 is not affective)			LFO FRQ		
R9	Only one for PSG }			LF TRG. LF CTL		

2.1.1 R0: Channel Select Register (ch SELECT)

Register R0, in conjunction with A0 – A3, controls the selection of specific register in a paticular channel. Register R2 – R7 are selected by A0 – A3 lines. Channel is specified by R0. (R0, R1, R8, R9 are selected directly by A0 – A3 lines.)

The configuration of register R0 is shown below.

	MSB 7	6	5	4	3	2	1	LSB 0
R0						ch SELECT		

The relation between the R0 value and the channel number is as follows. For example, R2 of ch3 is addressed by setting "2" in R0 and specifying "2" in A0 – A3.

The value of R0	0	1	2	3	4	5	6	7	(hexadecimal)
Channel	ch1	ch2	ch3	ch4	ch5	ch6			

2.1.2 R1: Main Amplitude Level Register (LMAL, RMAL)

This register controls the amplitude level of final sound (i.e, the mixture of channels). LMAL adjusts the level of the left-handed output (LOUT). RMAL adjusts the level of the right-handed output (ROUT). Maximum L/R amplitude level is obtained when "F" (hex) is set in LMAL/RMAL (4 bits of data). The output level is decreased about 3dB each time the register value is decreased by one.

	MSB 7	6	5	4	3	2	1	LSB 0
R1	LMAL				RMAL			

2.1.3 R2: Lower order of Frequency Register (FRQ LOW)

This 8-bit register, combined with R3, is used to determine the output frequency, and is lower order byte. (For frequency settings, see 2.3.)

	MSB 7	6	5	4	3	2	1	LSB 0
R2	FRQ LOW							

2.1.4 R3: Higher order of Frequency Register (FRQ HIGH)

The low-order four bits of R3 are used to determine the output frequency in conjunction with R2, and is higher order half byte.

	MSB 7	6	5	4	3	2	1	LSB 0
R3					FRQ HIGH			

2.1.5 R4: Channel On, Direct D/A, Channel Amplitude Level Register (ch ON, DDA, AL)

The MSB of this register (ch ON) controls the mixing of sound of the selected channel and the writing of data to the waveform register. The high-order second bit controls direct D/A. The low-order five bits controls the output level of the sound of the selected channel. (For details, see 2.1.7.)

	MSB 7	6	5	4	3	2	1	LSB 0
R4	chON	DDA		AL				

(1) Mode selection by ch ON, DDA bits

When the MSB is "1", the sound output of the selected channel is ON. When the bit is "0", the sound output goes off and data can now be written to the waveform register R6.

Direct D/A (DDA) mode is controlled by the high-order second bit. When this bit is "1", the address counter for the waveform register is reset and the DDA mode starts enabling data signals to be sent directly to the D/A converter.

chON	DDA	Mode	Operation
0	0	Write data mode	The waveform register address is incremented after a write cycle is completed.
0	1	Reset counter mode	The address counter for waveform register is reset.
1	0	Mixing (sound output) mode	The waveform register address is incremented under the timing resulted by the frequency register.
1	1	Direct D/A mode	The address counter is reset. In each write cycle, data is transferred to the D/A converter directly.

(2) Amplitude level adjustment

The low-order five bits (AL) defines the amplitude level of the sound of a channel. "$1F_{16}$" is maximum amplitude level. Each time the value decreases by one, the amplitude level decreases by about 1.5dB.

2.1.6 R5: LR Amplitude Level Register (LAL, RAL)

Register R5 controls the balance of amplitude level between the right-handed sound and the left-handed sound. LAL controls the amplitude level of the left-handed output; RAL controls that of the right-handed output. Maximum L/R amplitude level is obtained when each LAL and RAL is "F_{16}" (4 bits of data). Each time the register value decreases by one, the amplitude level decreases by 3dB.

	MSB							LSB
	7	6	5	4	3	2	1	0
R5	LAL				RAL			

2.1.7 R6: Waveform Register (WAVE DATA)

Register R6 stores waveform data. It contains 5 bits × 32 words of data per channel. The 32 words constitute one waveform cycle.

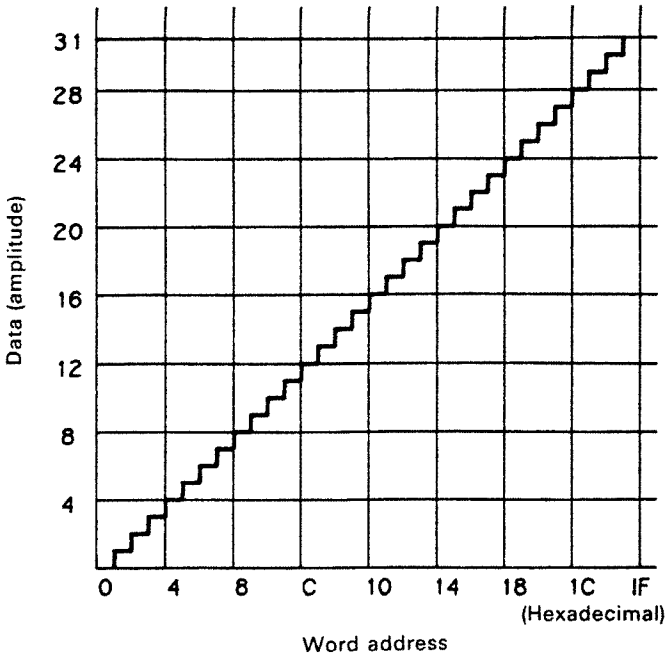
The configuration of register R6 is shown below:

	7	6	5	4	3	2	1	0	Internal address
R6				WAVE DATA					0
				↑					1
				↑					2
				↑					3
				⋮					⋮
				↑					$1D_{16}$
				↑					$1E_{16}$
				↑					$1F_{16}$

32 addresses

The relation between register data and waveform amplitudes (D/A converter output):

As shown, one cycle of sound is replaced with five bits of data in time series. In this example, the wave data is increased as wave address exceeds. (Saw wave)



■ Writing Wave Data

Refer to the information given in 2.1.5.

(1) Normal writing

Set ch ON = 0 and DDA = 0 (write data mode). Next, write the wave data to R6 of the selected channel (32 words) successively. Then, set ch ON = 1 and DDA = 0, to make sound. Do not forget to set MAL, AL, LAL and RAL. By this procedure of writing data, the start address of waveform register can not be specified.

(2) Specifing the start address of wave data

Set ch ON = 0 and DDA = 1, then ch ON = 0 and DDA = 0. This sets wave address counter to "0". Write 32 words of wave data continuously to R6. The data is stored sequentially at addresses $0\text{-}1F_{16}$. Set ch ON = 1 and DDA = 0, with setting up MAL, AL, LAL and RAL. Now sound is generated from the PSG.

(3) Direct D/A (DDA)

This mode allows wave data to be sent directly to the D/A converter. Before setting up in DDA mode set ch ON = 0 and DDA = 1, and write "00_{16}" to R6 (not to make sound) or set AL (R4) to 0. Then set ch ON = 1 and DDA = 1 so that this channel is ready to make sound directly. In each write cycle to R6, the data is transferred directly to the D/A converter and is hold untill next data come. (In this DDA mode, data in R6 are not changed.)

2.1.8 R7: Noise Enable, Noise Frequency Register (NE, NFRQ)

The MSB (NE) of register R7 selects noise or sound. When this bit is "1", noise is enabled and sound is disabled.

The low-order five bits are used to determine the frequency of clock signal to the noise generator. Greater the data higher the noise frequency. (See 2.3.3. noise frequency)

	MSB							LSB
	7	6	5	4	3	2	1	0
R7	NE			NOISE FRQ				

2.1.9 R8: Low-frequency Oscillator Frequency Register (LFO FRQ)

Register R8 combined with R2, R3 of ch.2 controls the L.F.O. frequency for frequency modulation. R8 and R2, R3 in ch.2 are extended into single divide-by-N counter to make Low Frequency. This LF proceeds the wave counter of ch.2 to form LF wave. (See following diagram) (For LFO frequency setting, see 2.3.2.)

	MSB							LSB
	7	6	5	4	3	2	1	0
R8	LFO FRQ							

2.1.10 R9: LFO Control Register (LF TRG, LF CTL)

(1) LF TRG

Writing "1" to the LF TRG bit (MSB) causes the LFO reset and initialization. And modulation is halted with modulation data from address "0" of waveform register of ch2. Wave counter is also reset to 0.

To start modulation, write "0" in the LF TRG bit.

(2) LF CTL

The low-order two bits (LF CTL) controls the degree of frequency modulation.

The frequency register pair (R3:R2) of ch.1 is modified by a value of R6 (ch.2) data. So, ch.1 output frequency is varied. LFO clock proceeds address counter of the R6.

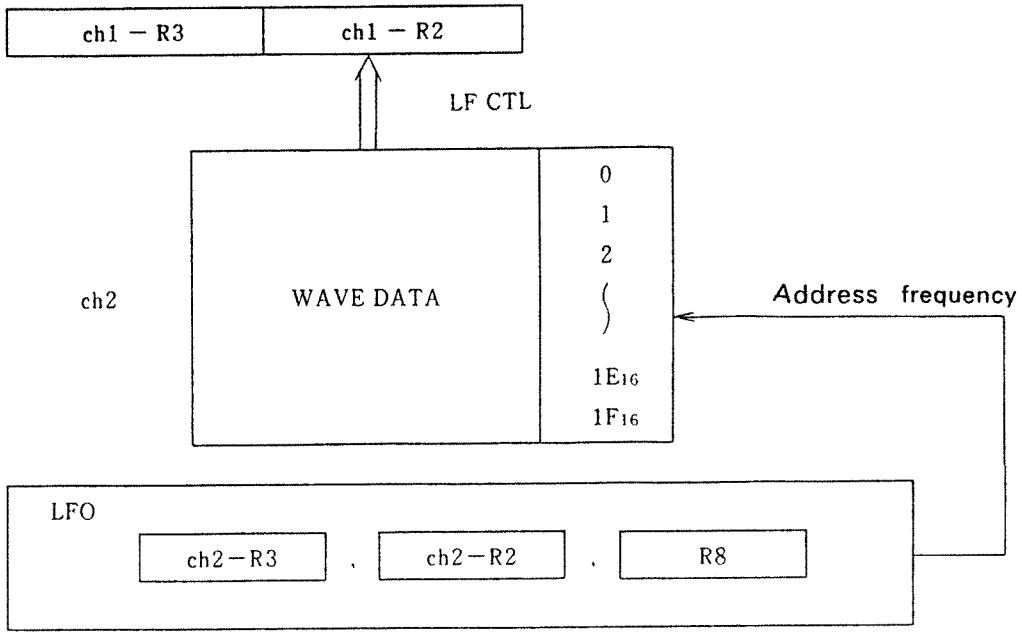
A new data to define frequency is obtained by addition of register pair and R6. LFCTL field defines bit location of this addition. And MSB of R6 is XSGN bit.

	MSB							LSB
	7	6	5	4	3	2	1	0
R9	LF TRG						LF CTL	

NOTE:

The LFO output is active only when both channel 1 and 2 are enabled. So, when LFO is active, the amplitude control register (AL or LAL, RAL) of channel 2 is also effective, ch.2 will produce a sound by LFO frequency, if ch.2 amplitude is enough.

■ LFO and Modulation



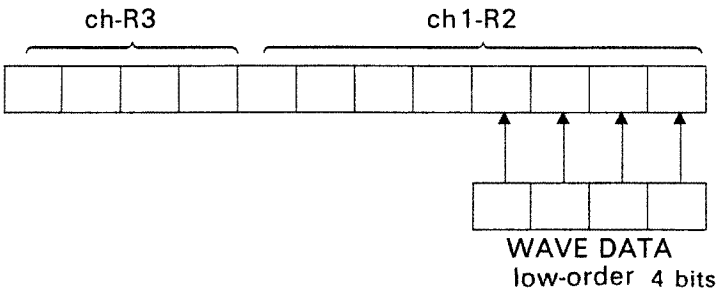
■ Waveform and corresponding value for modulation

Waveform value		Modulation value		Waveform value		Modulation value	
(binary)	(hex)	(hex)		(binary)	(hex)	(hex)	
11111	1F	+F	HIGH	01111	F	−1	HIGH
11110	1E	+E	↑	01110	E	−2	↑
11101	1D	+D		01101	D	−3	
11100	1C	+C		01100	C	−4	
11011	1B	+B		01011	B	−5	
11010	1A	+A		01010	A	−6	
11001	19	+9		01001	9	−7	
11000	18	+8		01000	8	−8	
10111	17	+7		00111	7	−9	
10110	16	+6		00110	6	−A	
10101	15	+5		00101	5	−B	
10100	14	+4		00100	4	−C	
10011	13	+3		00011	3	−D	
10010	12	+2		00010	2	−E	
10001	11	+1	↓	00001	1	−F	↓
10000	10	0	LOW	00000	0	−10	LOW

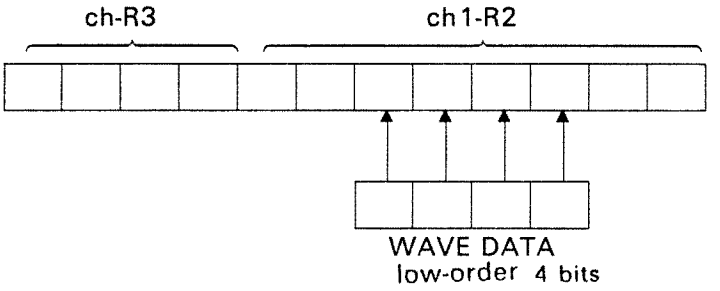
■ LF CTL bits

0	LFO is disabled
1	0 shift addition
2	2 bit shift left addition
3	4 bit shift left addition

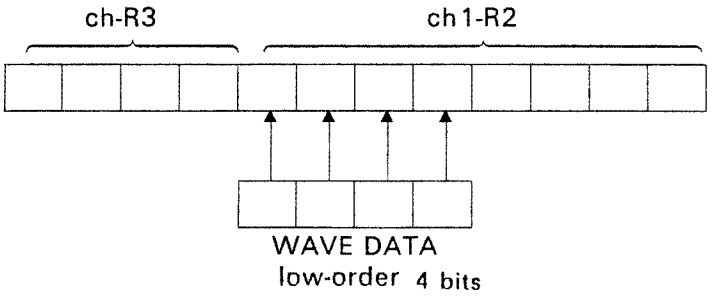
(A) LF CTL 1



(B) LF CTL 2



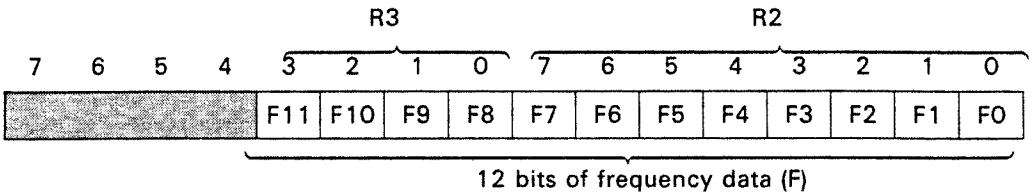
(C) LF CTL 3



2.2 Setup Frequencies

2.2.1 Waveform Output Frequency of each Channel

R2 and R3 of a channel determine its waveform output frequency. The relation between R2 and R3 data and frequencies is as follows:



R2 and R3 combine together to form 12 bits of frequency data (F).
The output frequency (f_{OUT}) is defined as:

$$f_{OUT} = \frac{fmaster}{(2 \times 32 \times F)}$$

where fmaster is the PSG driving clock frequency (7.16 MHz supplied by the CPU) and F is given in decimal notation (when calculated).

* F value "0" is forbidden.

2.2.2 LFO Frequency

The LFO frequency determines a frequency of frequency modulation. When the low-order two bits of the LF CTL register (R9) is 1, 2 or 3, LFO is effective.
The frequency counter of channel 2 and the LFO frequency counter are combined (20 bit length) together to generate an LFO frequency.
The LFO frequency (f_{LFO}) is defined as:

$$f_{LFO} = \frac{fmaster}{(2 \times 32 \times F_2 \times F_{LF})}$$

where F_2 is the F data (decimal) stored in R2 and R3 of channel 2 and F_{LF} is the data (decimal) in the LFO FRQ register.

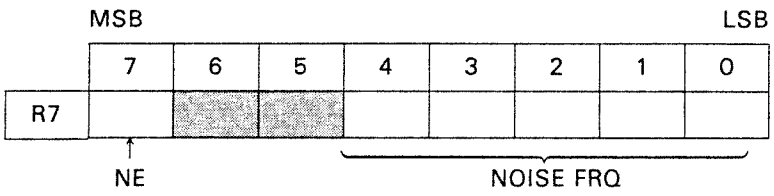
* f_{LFO} means the time interval to address the whole waveform data of channel 2 (32 words).

2.3.3 Setup Noise Frequency

R7 (noise frequency register) defines noise frequency.
This register defines the clock frequency of the noise generator:

$$f_{NCL} = \frac{fmaster}{(2 \times 32 \times 2 \times \overline{NF})}$$

where $\overline{NF}$ is the complement of 5 bits data of noise frequency register.
* When $\overline{NF} = 0$, f_{NCL} is undefined.



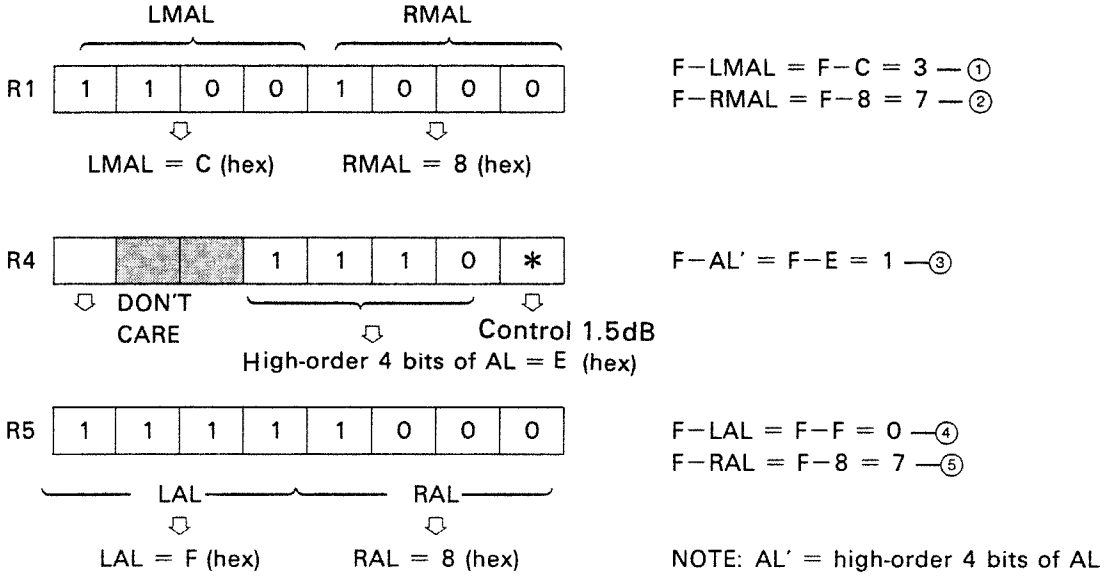
R7 is available for channel 5 and 6 only.

2.3 Amplitude Level Control

Amplitude level of sound output is controlled by the LMAL, RMAL register (R1), AL register (R4), and LAL, RAL register (R5). R4 and R5 exist for every channel, and control the output level of its sound. R1 controls the output level of mixed sound.

R1 and R5 varies the output amplitude level by 3dB steps, while R4 controls it by 1.5dB steps. For the HuC6280, however, its dynamic range is about 45dB (circuit design value) and none is output when the amplitude level decreases by 45dB from the maximum. (Actually, there may be a little leak output because of device characteristics.)

If R1, R4 or R5 of some channel is "0" or if the sum of the difference between R1/R5 and the high-order four bits of the AL register (the low-order five bits of R4) and value F_{16} (see below) exceeds F_{16}, then no sound is output from the channel.



For the left-handed sound, its amplitude level is 12dB lower than the maximum as calculated in the following:

① + ③ + ④ = 3 + 1 + 0 = 4

For the right-handed sound, its amplitude level is 45dB lower than the maximum as calculated in the following:

② + ③ + ⑤ = 7 + 1 + 7 = 15

In the latter case, no sound is generated.

R1 can be used to fade in/out the total sound or to move it to the right or left.

R4 can be used to control the output level or envelope of sound of a certain channel.

R5 can be used to control the balance of sound of a channel between right and left or to control the output level of sound of the channel.

2.4 Creating Waveform Data

Using a waveform observation device, such as an oscilloscope, make trace of waveform and convert it to digital data, typically, divide it by 32 horizontally and vartically. The waveform register containes 5 bits (amplitude data) × 32 words (time data, one cycle of waveform) memory each channel. For the procedure of writing data in the waveform register, see 2.1.7.

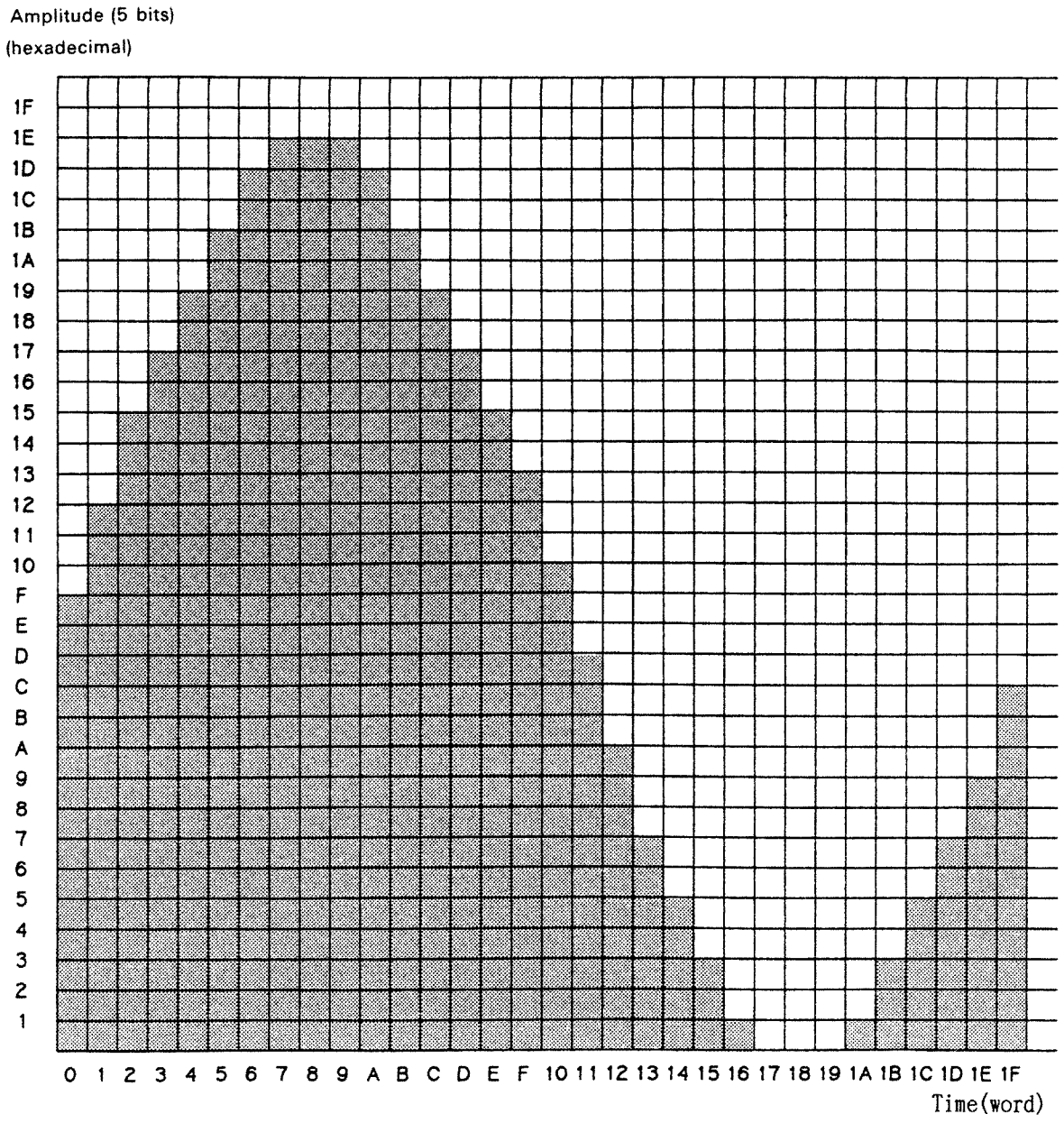


Fig. 2-4-1 Example of Sine Waveform Data Conversion

3. SCALE TABLE

Relation between equal temperament and PSG Output frequency (fmaster = 7.16 MHz)

Sound symbol	Frequency division ratio (decimal)	Register data R3 (hex)	Register data R2 (hex)	PSG output (Hz)	Equally tempered scale (Hz)	Sound symbol	Frequency division ratio (decimal)	Register data R3 (hex)	Register data R2 (hex)	PSG output (Hz)	Equally tempered scale (Hz)
C1	3,421	D	5D	32.70	32.70	A4	254	0	FE	440.45	440.00
C1#	3,229	C	9D	34.65	34.65	A4#	240	0	F0	466.15	466.16
D1	3,047	B	E7	36.72	36.71	B4	227	0	E3	492.84	493.88
D1#	2,877	B	3D	38.89	38.89	C5	214	0	D6	522.78	523.25
E1	2,715	A	9B	41.21	41.20	C5#	202	0	CA	553.84	554.37
F1	2,563	A	03	43.65	43.65	D5	190	0	BE	588.82	587.33
F1#	2,419	9	73	46.25	46.25	D5#	180	0	B4	621.53	622.25
G1	2,283	8	EB	49.00	49.00	E5	170	0	AA	658.09	659.26
G1#	2,155	8	6A	51.91	51.91	F5	160	0	A0	699.22	698.00
A1	2,034	7	F2	55.00	55.00	F5#	151	0	97	740.89	739.99
A1#	1,920	7	80	58.27	58.27	G5	143	0	8F	782.34	783.99
B1	1,812	7	14	61.74	61.73	G5#	135	0	87	828.70	830.61
C2	1,711	6	AF	65.39	65.40	A5	127	0	7F	880.91	880.00
C2#	1,615	6	4F	69.27	69.29	A5#	120	0	78	932.29	932.33
D2	1,524	5	F4	73.41	73.41	B5	113	0	71	990.4	987.77
D2#	1,438	5	9E	77.80	77.78	C6	107	0	6B	1,045.6	1,046.5
E2	1,358	5	4E	82.38	82.40	C6#	101	0	65	1,107.7	1,108.7
F2	1,282	5	02	87.27	87.30	D6	95	0	5F	1,177.6	1,174.7
F2#	1,209	4	B9	92.54	92.50	D6#	90	0	5A	1,243.1	1,244.5
G2	1,142	4	76	97.96	98.00	E6	85	0	55	1,316.2	1,318.5
G2#	1,077	4	35	103.88	103.83	F6	80	0	50	1,398.4	1,396.5
A2	1,017	3	F9	110.00	110.00	F6#	76	0	4B	1,472.0	1,480.0
A2#	960	3	C0	116.54	116.54	G6	71	0	46	1,575.7	1,568.0
B2	906	3	8A	123.48	123.47	G6#	67	0	43	1,669.8	1,661.2
C3	855	3	57	130.85	130.81	A6	64	0	40	1,748.0	1,760.0
C3#	807	3	27	138.63	138.59	A6#	60	0	3C	1,864.6	1,864.7
D3	762	2	FA	146.82	146.83	B6	57	0	39	1,962.7	1,975.7
D3#	719	2	CF	155.60	155.56	C7	53	0	35	2,110.8	2,093.0
E3	679	2	A7	164.76	164.81	C7#	50	0	32	2,237.5	2,217.5
F3	641	2	81	174.53	174.61	D7	48	0	30	2,330.7	2,349.3
F3#	605	2	5D	184.92	185.00	D7#	45	0	2D	2,486.1	2,489.0
G3	571	2	3B	195.93	196.00	E7	42	0	2A	2,663.7	2,637.0
G3#	539	2	1B	207.56	207.65	F7	40	0	28	2,796.9	2,793.8
A3	508	1	FC	220.23	220.00	F7#	38	0	26	2,944.1	2,960.0
A3#	480	1	E0	233.07	233.08	G7	36	0	24	3,107.6	3,136.0
B3	453	1	C5	246.96	246.94	G7#	34	0	22	3,290.4	3.322.4
C4	428	1	AC	261.39	261.63	A7	32	0	20	3,496.1	3,520.0
C4#	403	1	93	277.61	277.57	A7#	30	0	1E	3,729.2	3,729.3
D4	381	1	7D	293.64	293.66	B7	28	0	1C	3,995.5	3,951.1
D4#	360	1	68	310.76	311.13	C8	27	0	1B	4,143.5	4,186.0
E4	339	1	53	330.01	329.63						
F4	320	1	40	349.61	349.23						
F4#	302	1	2E	370.45	369.99						
G4	285	1	1D	392.54	392.00						
G4#	269	1	0D	415.89	415.30						