HuC6260

CMOS Video Color Encoder

MANUAL

TABLE OF CONTENTS

1. DESCRIPTION

The HuC6260 is a CMOS video color encoder (VCE) which has a sync signal generator, a color table RAM, an analogue RGB signal D/A converter and a video color-difference signal D/A converter integrated on one chip.
Through the color table RAM (color pallet), the HuC6260 converts video data received from the video display controller (VDC) into analogue RGB signals or video color-difference signals.

1.1 Features

- Monolithic CMOS video color encoder
- Built-in sync signal generator
- 512 different colors available (512 addresses on the color pallette)
- Two types of video signals are available:
  analogue RGB output signals and video color-difference signals
- Band width of the RGB signals: ... 7 MHz
- Capability for reading or writing data on the color pallette RAM
- A minimum number of external parts are needed to complete the composite video signal circuit
- Single 5V power supply (both for digital and analogue blocks)
- 80-pin plastic flat package

2. FUNCTIONS

2.1 Internal Registers

The HuC6260 contains internal registers. The CPU accesses these registers to set an operating mode, read/write color table RAM and perform other functions.

- Access to internal registers

  The CPU can access to each internal register only when the $\overline{CS}$ pin is at "L" level.

2.1.1 Control Registers

$\overline{CS}$	A1	A2	R/W	Sym-bol	Register name	A0													
						1								0					
						D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1																			
0	0	0	W	CR	Control Register									DCC					
0	1	0	W	CTA	Color Table Address									CTA					
0	0	1	W	CTW	Color Table Data Write									G			R		B
0	0	1	R	CTR	Color Table Data Read									G			R		B

- A0 specifies the low byte data when it is "0" and the high byte data when it is "1".

This can be summarized

- ▨ Shaded area

  The shaded area is not available.

2.1.2 Functions of Internal Registers

(1) Control Register (CR)

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								DCC							

The control register is used to specify a division ratio to the oscillator frequency from the OSC pin. A frequency-divided signal is outputted at the CK pin.
A division ratio of 4 is selected when the content of CR is "00_{16}", and 3 is selected when the content of CR is "01_{16}".
The relation between the oscillator frequency and clock frequency is shown below. Here, fsc is the color subcarrier frequency.

DCC	Frequency division ratio	f_{CLOCK}	fck
00_{16}	4	6fsc	1.5fsc
01_{16}	3	6fsc	2fsc

(2) Color Table Address Register (CTA)

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							CTA								

The color table address register holds an address pointing the internal color table RAM to where the CPU transfers data.
Once address data has been set into the CTA, the address data of the CTA is automatically incremented after a high byte data is transfered to the color table RAM. (In this case, an access to the high byte of data is the trigger of incrimenting the address data in the CTA.)

(3) Color Table Data Write Register (CTW)

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							G			R			B		

The CPU must write data into this register to change the content of the color table RAM.

(4) Color Table Data Read Register (CTR)

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							G			R			B		

The CPU must read data from this register to read the content of the color table RAM.

2.2 Color Table RAM (Color Pallette)

2.2.1 Organization of Color Table RAM

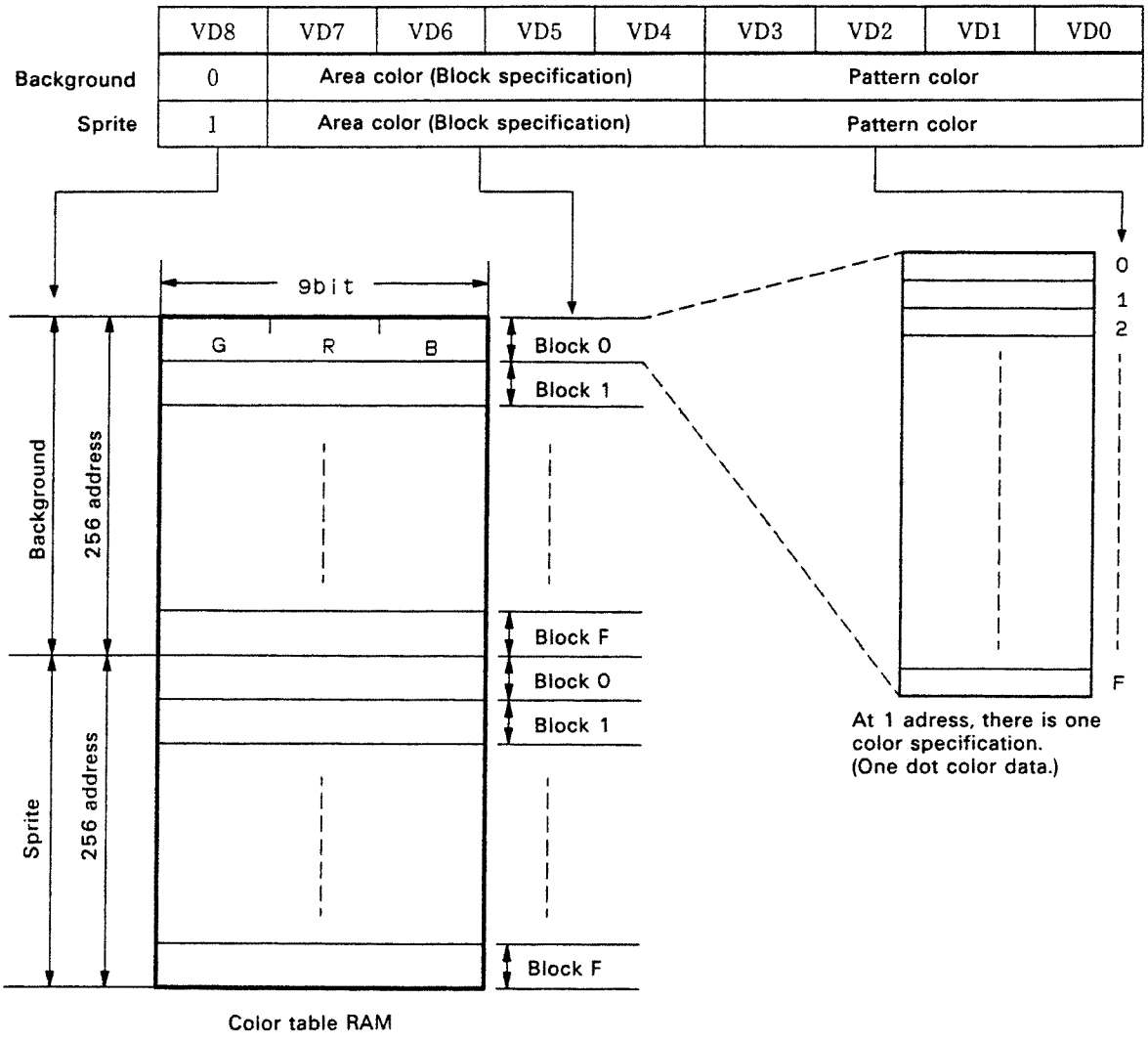

Fig. 2-2-1 Organization of Color Table RAM and its Relation with VD0-VD8

As shown in Fig. 2-2-1, the color table RAM is organized in 512 addresses x 9 bits of data to provide color informations.
There are 16 color blocks for background and sprite. And each color block has 16 pattern color informations.

2.2.2 Functions of Color Table RAM

In the color table, one address gives a information for one dot. Each 3 bits of the contents are shared for G, R and B information.

(1) Relation with CPU

The CPU writes a color data into the color table RAM. The CPU can read a color data from the color table RAM. (For the method of writing/reading data, see 2.2.2 -(3) Interface with the CPU.)

(2) Relation with VDC (Video Display Controller)

The relations with the color table RAM and each bit of digital color video signals (VD0-VD8) are shown below. (see Fig. 2-2-1)

- VD8 (SPBG for VDC)..... Specifies background or sprite
- VD7 – VD4 ..... Specifies a color block No.
- VD3 – VD0 ..... Specifies a pattern color No.

The HuC6260 produces color image signal to the CRT from digital video data according to the above specification.

This addressing method allows the 512 addresses to be grouped into two 256-address areas, each of which is divided into 16 blocks. Each block has 16 addresses for pattern color informations.

(3) Interface with CPU

(a) Writing data into color table RAM

Step 1: Write the low byte of the starting address into the color table address register (CTA).

Step 2: Write the high byte of the starting address into the color table address register (CTA).

Step 3: Write the low byte of the data into the color table RAM.

Step 4: Write the high byte of the data into the color table RAM.
(After this step, address data in CTA is incremented automatically.)

(b) Reading data from color table RAM

Set the starting address and read the data. (The accessing procedure needs two steps both for writing the address data and for reading a data, first step for low byte and second step for high byte. CTA is incremented after the access of high byte of data.)